RELIABLE IMPLEMENTATION OF SERIAL PSEUDORANDOM/NATURAL CODE CONVERTER

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Abstract

Serial pseudorandom/natural code converters are used in pseudorandom absolute position encoders and participate significantly in the total time required to determine the absolute position. The paper presents an improved and reliable implementation of serial converter with reduced conversion time by simultaneously activating two PRBS generators based on direct and reverse generation law. A basic serial pseudorandom/natural code converter based on an PRBS generator with reverse generation law, as well as presented converter, are implemented using LabVIEW FPGA software and R series multifunction acquisition card PCIe-7841R with Virtex-5 LX30 FPGA. The presented serial converter has significantly less conversion time, but a slightly more complex implementation.

Keywords: pseudorandom/natural code converter, absolute pseudorandom position encoder, LabVIEW FPGA

INTRODUCTION

The pseudorandom absolute position encoders are digital transducers used for angular position determination which is needed in many industrial applications. Accurate, reliable and fast measurement of angular position can directly affect the quality of the end products in the industry. These encoders use properties of n-bit pseudorandom binary sequence (PRBS), and most of all, if *n* adjacent bits are read, a code word that has a unique position is obtained [1, 2]. Also, compared to conventional absolute encoders, these encoders enabled the use of a smaller number of code reading sensors due to a smaller number of code tracks, as well as the application of detection methods for reading code errors. Then these encoders can be designed to be easier to mount on the motor shaft. They can be applied in industry for motorized linear stages, robotics, computer peripherals, antennas, etc.

Functioning of the encoder would not be possible without the following constituent components: code reading, code scanning, pseudorandom/natural code conversion and code reading error detection. Code reading of longitudinally arranged pseudorandom binary code can be realized serial using one [1] or two [4] code reading heads, or in parallel using sensor array. Very important for reading the pseudorandom code is the accurate and reliable definition of the reading moment, and this can be realized in different ways, but usually synchronization track is added next to the code track [5]. The pseudorandom code has enabled the application of various methods for detecting code reading errors that can be exploited to increase the reliability of the encoder itself. In order to obtain a natural code that is easier to handle in digital electronics, conversion of pseudorandom / natural code is required.

The conversion of the pseudorandom into a natural code can be implemented using three methods: parallel [2], serial [1, 6] and combined serial-parallel [8]. The serial conversion is the hardware simplest, but the conversion time is the longest. On the other hand, the parallel conversion is the fastest but hardware expensive, as it requires large memory elements for high-resolution encoders. Serial-parallel conversion is a compromise solution that combines the previous two methods and the hardware is the most complex.

The first part of the paper describes a basic serial converter based on the Fibonacci generator of PRBS with reverse generation law on the example of an 8-bit pseudorandom binary code. An upgraded serial converter solution that uses two Fibonacci PRBS generators, one with direct and the other with reverse generation law, is then described. Both solutions are implemented in the FPGA device using LabVIEW FPGA software. Finally, the properties of realized serial pseudorandom/ natural code converters are discussed and their advantages and disadvantages are highlighted.

SERIAL PSEUDORANDOM/ NATURAL CODE CONVERTER WITH FIBONACCI GENERATOR

The serial pseudorandom/natural code converter is based on the application of the PRBS Fibonacci generator with appropriate feedback for reverse generation law and counting the steps necessary to reach the initial state. The higher the resolution of the code, the required number of steps for converting any read code word increases. The serial converter based on Fibonacci generator of PRBS for resolution of n = 8 is shown in Fig. 1. A 255 bits long pseudorandom binary sequence is obtained by Fibonacci generator with feedback set for direct generation law [6, 5, 4, 0]. There must be an assembly register to form a code word based on the read bits from pseudorandom code track. The formed code word is after each read bit loaded into shift register of Fibonacci generator. The feedback sets for any resolution can be found in the literature [7]. The 8-bit counter is used to count the necessary number of steps for one conversion cycle. The additional logic for initial state $X(0)$ identification is also needed.

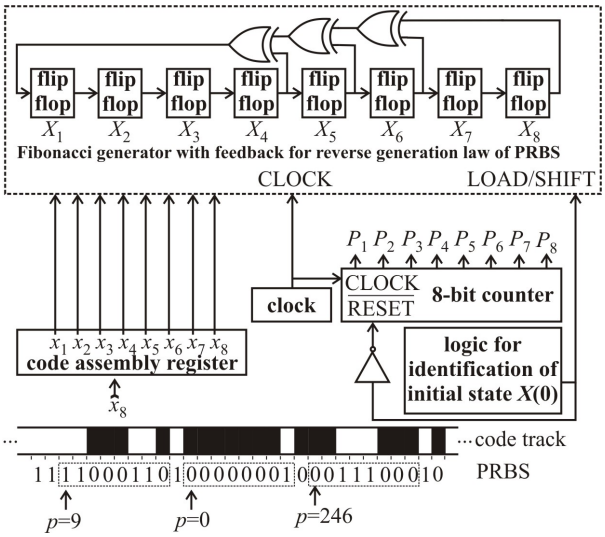

Fig. 1. *Serial pseudorandom/natural converter based on Fibonacci generator*

This serial pseudorandom / natural code converter is implemented in the LabVIEW FPGA software, compiled and executed in hardware, that is, in the FPGA device of the PCIe-7841R card, Fig. 2. In the block diagram, there are additional circuits for measuring conversion times that are not necessary in the final encoder realization. In this converter, the Fibonacci generator of PRBS is consisted from the 8-bit shift register with reverse XOR feedback configuration according to feedback set [7, 5, 4, 3] for reverse generation law. LabVIEW FPGA implementation is easier to design, can be easily modified and upgraded, compared to using VHDL programming. The compilation process for FPGA devices can last minutes to hours.

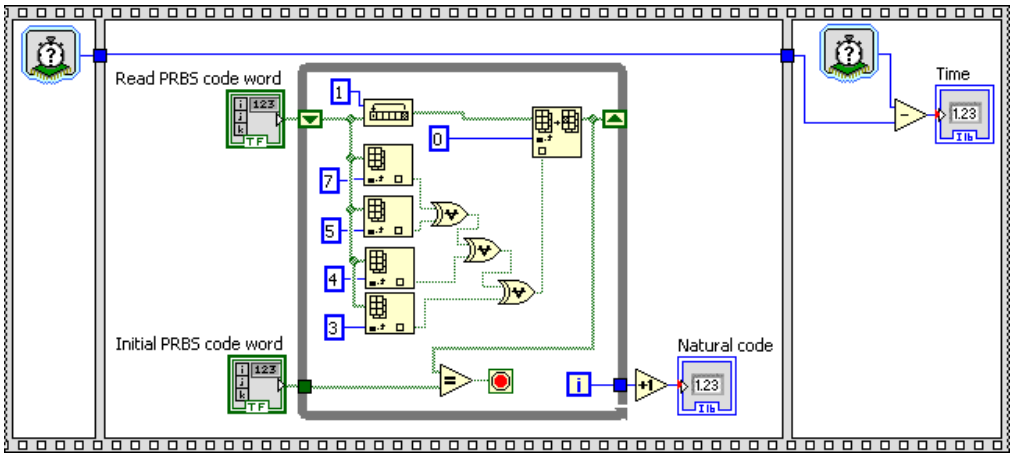

Fig. 2. *Serial pseudorandom/natural converter in LabVIEW FPGA*

One technique to reduce the amount of compilations is to simulate application on the development computer and resolve any programming errors before going to hardware.

UPGRADED SERIAL PSEUDORANDOM/ NATURAL CODE CONVERTER

Presented serial pseudorandom/natural code converter is based on the application of two Fibonacci generators of PRBS with direct and reverse generation law, Fig. 3. In both generators, the read code word is loaded at the start of the conversion process, and then the generator that first reaches to the initial code word ends the conversion process. In this way, the conversion time is reduced approximately twice. Also, in this realization are needed register for forming of read code word, 8-bit counter, and logic for identification of initial state. In this particular example of the 8-bit code, there are 255 positions, or 255 different code words. When obtained position is greater than 2^{n-1}-1 = 2^7-1=127, generator with feedback for direct generation law will first reach the initial state. On the other hand, if the position is less than 127, the initial state will first reach the generator with feedback for reverse generation law.

This upgraded serial pseudorandom /natural code converter is also implemented in LabVIEW FPGA and its functionality and properties are tested in hardware, Fig. 4. This converter utilizes 911 slice registers and 956 slice LUTs in FPGA device, compared to basic serial converter which utilizes 836 slice registers and 872 slice LUTs.

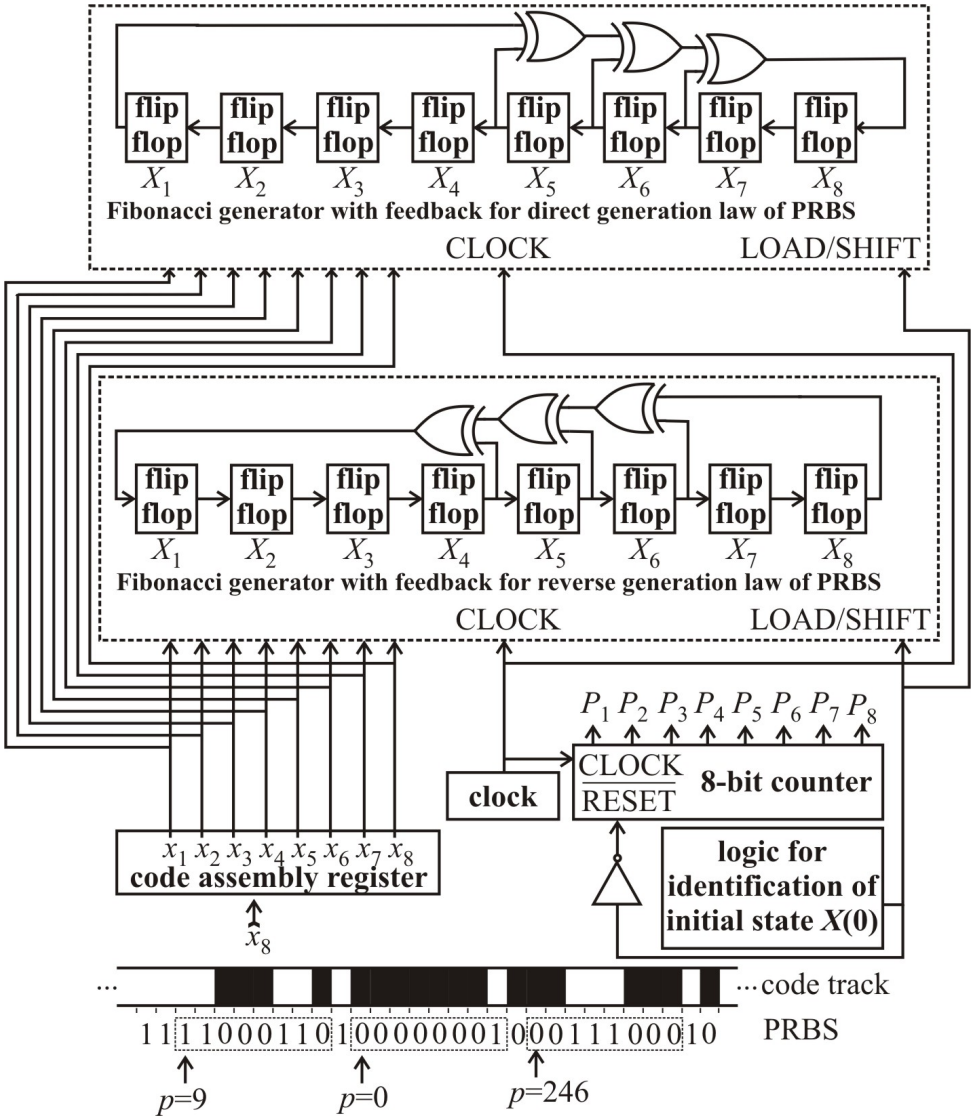

Fig. 3. *Upgraded serial pseudorandom/natural code converter*

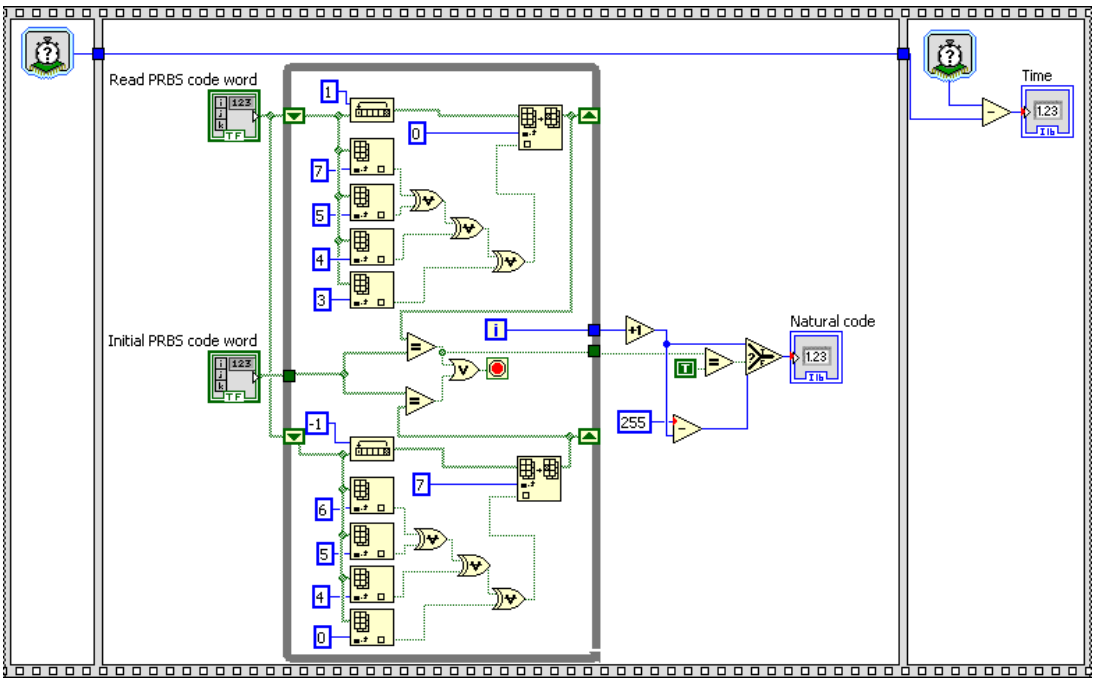

Fig. 4. *Upgraded serial pseudorandom/natural converter in LabVIEW FPGA*

For the initial code word is used 10000000, and converter are tested for the read code words 01100011 (P=9) and 00011100 (P=246). For both of these positions, the upgraded serial converter gives the same conversion time of 4 μs. On the other hand, the serial converter of Fig. 2 gives for the position 9 the conversion time 2 μs, and for position 246 the conversion time is 74 μs. A significant decrease in conversion time in case of position 246 can be seen.

CONCLUSION

Two different implementations of serial pseudorandom/natural code converters are presented and implemented in hardware, FPGA device. The upgraded serial converter has much better features regarding the conversion time compared to the basic version, but it is a bit more complex in hardware. Converters are implemented using LabVIEW FPGA and PCIe-7841R card to test functionalities and features.

ACKNOWLEDGEMENT

Research activities presented in this paper, are supported by funds of the Serbian Ministry of Education, Science and Technological Development, having the reference project number TR32045.

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