UNITECH 2017 GABROVO

INTERNATIONAL SCIENTIFIC CONFERENCE
17-18 November 2017, GABROVO

DTMOS BASED LOW POWER LOW VOLTAGE INDUCTANCE SIMULATOR

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Abstract
In this paper, a low voltage and low power inductance simulator based on dynamic threshold voltage MOS transistors is proposed. The proposed inductance simulator circuit is operating at 0.15 V power supply and due to the use of DTMOS transistors, the power consumption of the circuit has been reduced considerably compared to the conventional circuit as 7.65 μW. Also a band-pass filter structure is presented as an application of the proposed inductance simulator. The simulations of the inductance simulator and band-pass filter are performed with LTSPICE using 0.18 μm TSMC CMOS process. The simulation results are given to confirm of the theoretical analysis.

Keywords: DTMOS, inductance simulator, low voltage, low power.

INTRODUCTION

Passive spiral inductors are used in a wide range of application in RF systems such as filtering, impedance matching, phase shifting, biasing, designing oscillators etc. However, on-chip inductors realized by passive spiral inductors have some disadvantages such as large silicon area, low quality factor and limited inductance value. For these reasons, MOS transistor based inductance simulators are mostly used instead of passive spiral inductors. CMOS inductance simulators provide the advantages as small chip area, high quality factor, tunability, large inductance value, low noise and power consumption [1]. Also, power consumption can be further reduced by using DTMOS.

In the technical literature, there are several inductance simulators using CMOS based active elements such as dual-X second-generation current conveyor (DXCCII) [2]-[3], current feedback operational amplifier (CFOA) [4], current differencing transconductance amplifier (CDTA) [5], differential difference current conveyor (DDCC) [6], voltage differencing buffer amplifier (VDBA) [7]-[9], voltage differencing current conveyor (VDCC) [10], Z-Copy voltage differencing transconductance amplifier (ZC-VDTA) [11], second generation differential current conveyor (DCCII) [12], operational transresistance amplifier (OTRA) [13], current differencing current conveyor (CDCC) [14], voltage differencing transconductance amplifier (VDTA) [15], voltage differencing inverting buffered amplifier (VDIBA) [16] have been proposed. Likewise, inductance simulators using MOS transistors and passive components [17]-[18] and only MOS inductance simulators [19]-[20] have been reported.

The goal of this paper is to present a low voltage, low power inductance simulator. Only two DTMOS transistors and one biasing current are used to realize the proposed circuit. Thanks to using DTMOS transistors, the power consumption of the circuit is lower. Also, a second order band pass filter structure is proposed in order to verify the versatility of using inductance simulator. Proposed DTMOS based inductance simulator and band pass filter structures are simulated in LTSPICE by using 0.18 μm TSMC CMOS process.

DTMOS BASED INDUCTANCE SIMULATOR

Assaderaghi and others proposed the Dynamic Threshold voltage MOSFET

(DTMOS) to extend the lower bound of power supply to ultra-low voltages [21]. Their proposed DTMOS has a high threshold voltage at zero bias and low threshold voltage at $V_{gs}=V_{dd}$. The body terminal of the transistor is tied to gate terminal to generate the DTMOS transistor. DTMOS was proposed for obtaining excellent subthreshold characteristics at ultra-low V_{dd} [22]–[23]. Although PMOS transistors can be connected easily as DTMOS transistor, NMOS transistors require triple-well process which is very expensive processes to produce DTMOS transistor with their own wells. Only PMOS transistors are used as a DTMOS in this study. The transistors in this circuit are biased in weak inversion where a MOS transistor's drain current is given by

$$I_D = I_S\left(\frac{W}{L}\right)\exp\left(q\frac{V_{GS}-V_{TH}}{nkT}\right)\left[1-\exp\left(-q\frac{V_{DS}}{kT}\right)\right] \quad (1)$$

If $V_{DS} \geq 3kT/q$, strong inversion operation and high frequency applications are not possible using this circuit because the transistor will saturate in weak inversion [23]. The transconductance gm is described by

$$g_m = q\frac{I_D}{nkT} \quad (2)$$

The circuit symbol of DTMOS transistor is shown in Fig. 1 [24]. The proposed DTMOS based inductance simulator is shown in Fig. 2. A dynamic threshold technique is applied in both of the transistors M_1 and M_2.

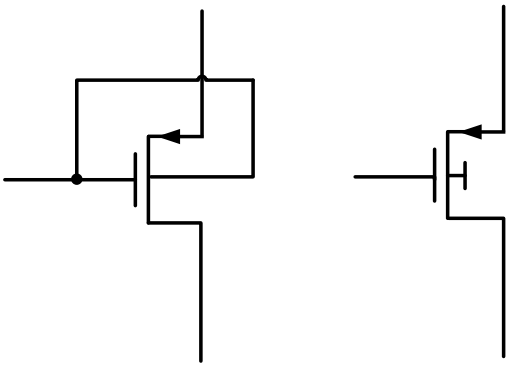

Fig. 1. *DTMOS transistor and its circuit symbol [24].*

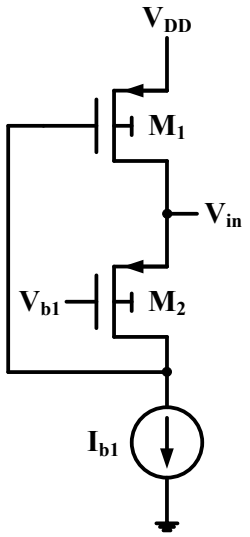

Fig. 2. *The proposed DTMOS based inductance simulator.*

The proposed inductance simulator given in Fig. 2 is simulated with LTSPICE using 0.18 µm TSMC CMOS process with 0.15 V supply voltage. The dimensions of the transistors are chosen as W_1/L_1=72/0.45 µm and W_2/L_2=44/0.45 µm. The terminal V_{b1} is used to provide DC voltage bias for transistor M_2 as -0.48 V and the value of the biasing current I_{B1} is taken as 60 µA. The power consumption of the proposed inductance simulator has decreased due to the use of DTMOS transistors. Reduction in the power supply and power consumption are useful for low power applications.

The simulated frequency responses of the proposed inductance simulator is shown in Fig. 3. The inductance value of the inductance simulator is 320 nH and it can be used between 20 MHz to 400 MHz frequency range.

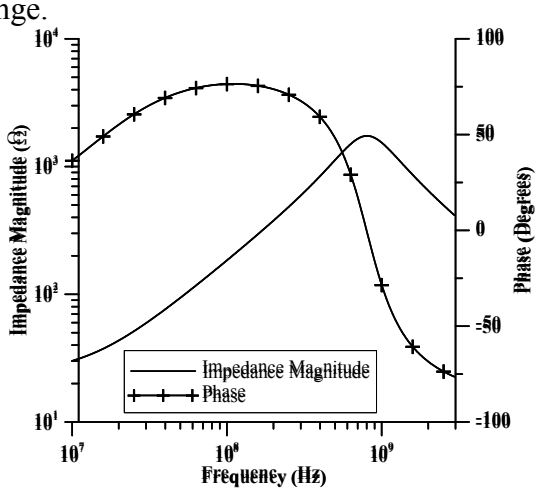

Fig. 3. *Frequency responses of the proposed inductance simulator.*

The performance of the proposed DTMOS based inductance simulator is demonstrated in an example of second order band-pass filter structure as shown in Fig. 4. For the presented band-pass filter, the passive components are selected as R_1=500 Ω and C_1=3.95 pF and L_{eq1}=320 nH, which is the inductance value of the proposed inductance simulator given in Fig. 2. The center frequency of the filters are calculated as f_0=150 MHz. Both ideal and simulated second order band-pass filter frequency responses are shown in Fig. 5. It can be seen that the frequency responses of ideal and inductor simulator based filters are in a good agreement.

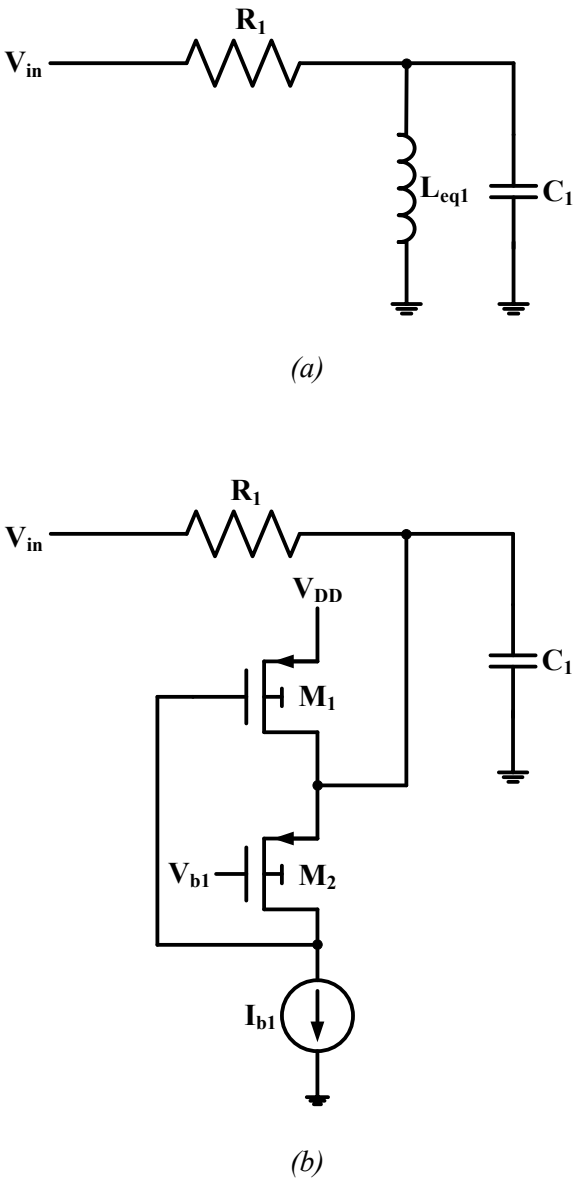

Fig. 4. *Second order band pass filter structures (a) Ideal filter (b) Inductance simulator based filter.*

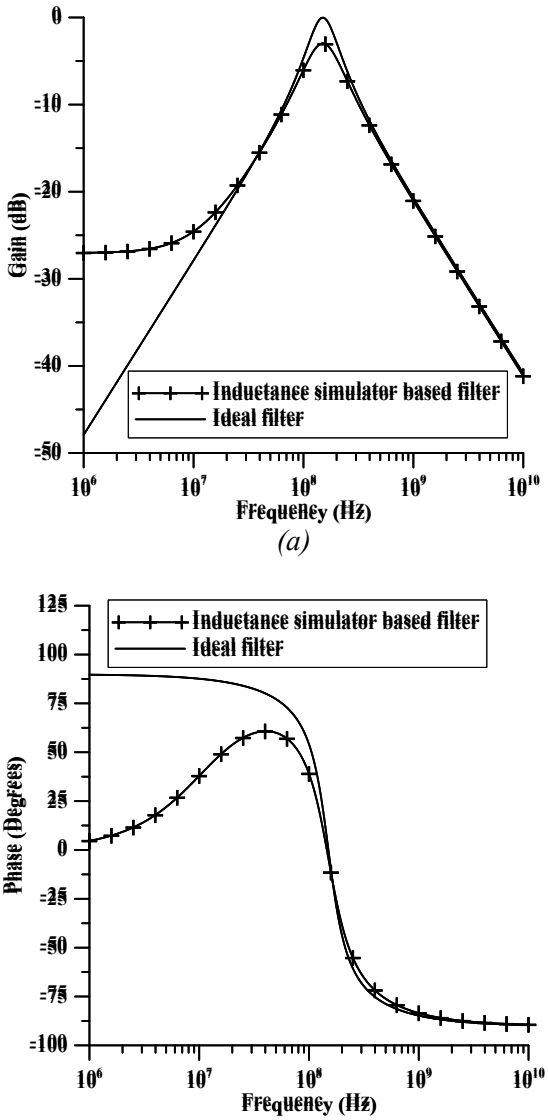

Fig. 5. *Frequency responses of the band pass filters (a) Gain (b) Phase.*

CONCLUSION

In this paper a DTMOS based inductance simulator is presented. It contains two DTMOS transistors and one biasing current. Passive components are not used in the proposed inductance simulator so it is attractive for integrated circuit implementations. Also, the inductance simulator provides advantages as low power supply and power consumption. In order to verify the practicality of using inductance simulator in RF filters, a second order band pass filter structure is designed. The simulation results of the inductance simulator and band pass filter are demonstrated with LTSPICE using TSMC 0.18 μm CMOS process. The simulation results agree well with the theoretical analysis.

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